<u>Claims</u>

What is claimed is:

1 1.   An arithmetic circuit comprising:
2   a plurality of registers;
3   an arithmetic unit, for regarding, as inputs, values entered in said
4   multiple registers; and
5   a plurality of memories, wherein reading of multiple variables from said
6   plurality of memories to said plurality of registers is performed during
7   the same reading cycle by way of a pipeline process performed by said
8   arithmetic unit.

1 2.   The arithmetic circuit according to claim 1, wherein said arithmetic unit is
2   a multiplier adder for, based on values x_1, x_2, x_3 and x_4 having an r-bit
3   length that are respectively input to a first register, second register, third
4   register and fourth register, providing a result Q for $x_1 + x_2 \cdot x_3 + x_4$ having
5   a length of 2r bits or 2r+1 bits.

1 3.   The arithmetic circuit according to claim 2, wherein said multiple
2   memories include a first memory and a second memory; and wherein, at
3   a stage for writing an operation result, which follows the operation stage
4   of said pipeline process, lower r bits Q_L of said operation result Q are
5   recorded in said first memory, and upper bits Q_H of said operation result
6   Q, excluding said bits Q_L, are recorded in said fourth register, while at a
7   stage for reading variables from said registers, which follows said writing
8   stage, simultaneously, a variable x_1 is read from said first memory and is
9   stored in said first register, and a variable x_3 is read from said second
10   memory and is stored in said third register.

1 4. The arithmetic circuit according to claim 3, wherein said first memory
2 and said second memory are two-port memories having one data writing
3 port and one data reading port.

1 5. The arithmetic circuit according to claim 3, wherein said first memory is
2 a two-port memory having one data writing port and one data reading
3 port, while said second memory is a single-port memory having one port
4 for the writing and reading of data.

1 6. The arithmetic circuit according to claim 1, wherein said arithmetic unit is
2 a multiplier adder for, based on values x_1, x_2, x_3, x_4 x_5 and x_6, having an
3 r-bit length, that are respectively input to a first register, a second
4 register, a third register, a fourth register, a fifth register and a sixth
5 register, and for providing the operation results Q for $x_1 + x_2 \cdot x_3 + x_4 \cdot x_5 +$
6 x_6, which have a length of 2r bits or 2r+1 bits.

1 7. The arithmetic circuit according to claim 6, wherein said multiple
2 memories include a first memory, a second memory and a third memory;
3 wherein, at a stage for writing an operation result, which follows the
4 operation stage of said pipeline process, lower r bits Q_L of said operation
5 result Q are recorded in said first memory, and upper bits Q_H of said
6 operation result Q, excluding said bits Q_L, are recorded in said sixth
7 register; and wherein, at a stage for reading variables to said registers,
8 which follows said writing stage, simultaneously, a variable x_1 is read
9 from said first memory and is stored in said first register, a variable x_3 is
10 read from said second memory and is stored in said third register, and a
11 variable x_5 is read from said third memory and is stored in said fifth
12 register.

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1   8.   The arithmetic circuit according to claim 7, wherein said first memory is
2   a two-port memory having one data writing port and one data reading
3   port, and said second memory and said third memories are single-port
4   memories having one port for the writing and the reading of data.

1   9.   An arithmetic method using an arithmetic circuit that includes an
2   arithmetic unit, which has multiple input registers and multiple memories,
3   comprising the steps of:
4   performing an arithmetic operation based on values stored in said
5   input registers;
6   writing the results of said arithmetic operation in said input
7   registers or said memories; and
8   reading multiple variables from said multiple memories and
9   storing said variables in said multiple input registers during the
10   same pipeline stage.

1   10.   The arithmetic method according to claim 9, wherein said arithmetic unit
2   is a multiplier adder for, based on values x_1, x_2, x_3 and x_4 having an r-bit
3   length that are respectively input to a first register, a second register, a
4   third register and a fourth register, providing the operation results Q for
5          $x_1 + x_2 \cdot x_3 + x_4$ having a length of 2r bits or 2r+1 bits.

1   11.   The arithmetic method according to claim 10, wherein said multiple
2   memories include a first memory and a second memory, further
3   comprising:
4   a writing step in a pipeline process of said arithmetic unit for
5   recording, in said first memory, lower r bits Q_L of said operation
6   result Q, and for recording, in said fourth register, upper bits Q_H of
7   said operation result Q, excluding said bits Q_L; and

8   a reading step of performing, at the same reading stage in said

9   pipeline process, the reading of a variable x_1 from said first

10   memory and storing said variable x_1 in said first register, and the

11   reading of a variable x_3 from said second memory and storing

12   said variable x_3 in said third register.

1   12.   The arithmetic method according to claim 11, wherein said first memory

2   and said second memory are two-port memories having one data writing

3   port and one data reading port.

1   13.   The arithmetic method according to claim 11, wherein said first memory

2   is a two-port memory having one data writing port and one data reading

3   port, while said second memory is a single-port memory having one port

4   for the writing and reading of data.

1   14.   The arithmetic method according to claim 9, wherein said arithmetic unit

2   is a multiplier adder for, based on values x_1, x_2, x_3, x_4 x_5 and x_6, having

3   an r-bit length, that are respectively input to a first register, a second

4   register, a third register, a fourth register, a fifth register and a sixth

5   register, and for providing the operation results Q for $x_1 + x_2 \cdot x_3 + x_4 \cdot x_5 +$

6   x_6, which have a length of 2r bits or 2r+1 bits.

1   15.   The arithmetic method according to claim 14, wherein said multiple

2   memories include a first memory, a second memory and a third memory,

3   further comprising:

4   a writing step in a pipeline process of said arithmetic unit for

5   recording, in said first memory, lower r bits Q_L of said operation

6   result Q, and for recording, in said sixth register, upper bits Q_H of

7   said operation result Q, excluding said bits Q_L; and

8		a reading step of performing, at the same reading stage of said
9		pipeline process, the reading of a variable x_1 from said first
10		memory and storing said variable x_1 in said first register, the
11		reading of a variable x_3 from said second memory and storing
12		said variable x_3 in said third register, and the reading of a variable
13		x_5 from said third memory and storing said variable x_5 in said fifth
14		register.

1	16.	The arithmetic method according to claim 15, wherein said first memory
2		is a two-port memory having one data writing port and one data reading
3		port, while said second and third memories are single-port memories
4		having one port for the writing and reading of data.

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